CLAIMS

1. A system for enabling communication between a first network having a first network protocol and a second network having a second network protocol, at least one of said first and second networks being a storage area network, said system comprising:

a first data port for receiving input data from said first network said input data being expressed in said first network protocol;

a second data port for receiving state information indicative of a state of a first storage area network selected from said first and second networks; and

a microsequencer system configured to translate said input data on the basis of said state information, said microsequencer system translating said input data into corresponding data expressed in said second network protocol.

2. The system of claim **1**, wherein said microsequencer system comprises at least one programmable microsequencer.

3. The system of claim **1**, wherein said microsequencer system comprises a microsequencer.

4. The system of claim **1**, wherein said microsequencer system comprises a plurality of microsequencers configured to cooperate in translating said input data into corresponding data expressed in said second network protocol.

5. The system of claim **1**, further comprising:

an instruction memory accessible to a constituent microsequencer of said microsequencer system, said instruction memory having a plurality of instruction words, each of said instruction words having sufficient length to hold at least two instructions; and

an instruction-memory pointer for identifying a selected instruction word in said instruction memory.

6. The system of claim **4**, further comprising a translation-memory accessible to a

constituent microsequencer of said microsequencer system, said translation-memory having

a translation-memory address , and

a translation-memory element corresponding to said translation-memory address, said translation-memory element including data for causing said instruction-memory pointer to jump to said selected instruction word.

7. The system of claim **6**, wherein said translation-memory element is configured to include an absolute address of said selected instruction word.

8. The system of claim **6**, wherein said translation-memory element is configured to include an offset from a current instruction word to said selected instruction word.

9. The system of claim **6**, further comprising a translation-memory pointer for indirectly causing said instruction-memory pointer to jump to a selected instruction-memory address.

10. The system of claim **9**, wherein said translation-memory pointer is configured to identify a selected translation-memory address corresponding to a translation-memory element that contains data indicative of said selected instruction-memory address.

11. The system of claim **4**, further comprising a translation-memory having:

a translation-memory address ;

a first translation-memory element corresponding to said translation-memory address, said first translation-memory element including data for causing said instruction-memory pointer to jump to a first instruction word;

a second translation-memory element corresponding to said translation-memory address, said second translation-memory element including data for causing said instruction-memory pointer to jump to a second instruction word; and

a selector for selecting said first translation-memory element.

12. The system of claim **11**, wherein said selector comprises a multiplexer having

a first multiplexer input for receiving data indicative of content of said first translation-memory element;

a second multiplexer input for receiving data indicative of content of said second translation-memory element;

an output providing data selected from at least said first multiplexer input and said second multiplexer input; and

a control input for controlling data provided at said output.

13. The system of claim **1**, further comprising an output port in communication with said microsequencer system for providing said corresponding data to said second network.

14. The system of claim **1**, wherein said first and second data ports and said microsequencer system are integrated into one integrated circuit.

15. A system for enabling communication between a first network having a first network protocol and a second network having a second network protocol, said system comprising:

a first input port for receiving input data from said first network;

a second input port for receiving state information associated with said first network;

a processing element in communication with said first and second input ports;

an instruction memory accessible to said processing element, said instruction memory having a plurality of instruction words, each of said instruction words having sufficient length to hold at least two instructions, said plurality of instruction words being selected to translate input data from said first protocol to said second protocol; and

an instruction-memory pointer for identifying a selected instruction word in said

instruction memory.

16. The system of claim **15** wherein said processing element is selected from the group consisting of: a microsequencer system having at least one microsequencer; a micro-processor; and an application-specific integrated circuit.

17. A processing system comprising:

a processing element ;

an instruction memory accessible to said processing element, said instruction memory having an associated instruction-memory pointer for identifying a selected instruction word in said instruction memory; and

a translation-memory accessible to said processing element, said translation-memory having a translation-memory element identified by a translation-memory address , said translation-memory element including data for causing said instruction-memory pointer to jump to said selected instruction word.

18. The processing system of claim **17**, further comprising a translation-memory pointer for indirectly causing said instruction-memory pointer to jump to a selected instruction-memory address.

19. The processing system of claim **18**, wherein said translation-memory pointer is configured to identify a selected translation-memory address that corresponds to a translation-memory element containing data indicative of said selected instruction-memory address.

20. The processing system of claim **17**, wherein said translation-memory element is configured to include an absolute address of said selected instruction word.

21. The processing system of claim **17**, wherein said translation-memory element is configured to include an offset from a current instruction word to said selected instruction word.

22. The processing system of claim **17**, wherein said instruction memory includes a plurality of instruction words, each of said instruction words having sufficient

length to hold at least two instructions.

23. The processing system of claim **17**, wherein said processing element is selected from the group consisting of a microsequencer system having at least one microsequencer, a microprocessor, a microcontroller, and an application-specific integrated circuit.